Engineering College, Ajmer,
N.H.8 , Barliya Circle, Near Nareli Temple, Ajmer

ECA/TEQIP-III/2019/193 **PURCHASE ORDER** 26/12/2019

Package Code: TEQIP-III/2019/RJ/GECA/100 **Current Date: 20-Dec-2019**

Package Name: GECA/TEQIP-III/2019-20/EIC- Digital System Design Lab **Method:Shopping Goods**

PO Reference No : TEQIP-III/2019/RJ/geca/100
Date of Issue: 20-Dec-2019
Subject : GECA/TEQIP-III/2019-20/EIC- Digital System Designing Lab

Purchaser : Engineering College, Ajmer,N.H.8 , Barliya Circle, Near Nareli Temple, Ajmer

Supplier Name: Vinytics Peripherals Pvt. Ltd.,
12-DDA, Auto Mobile Market (Truck Market) Opp. R. K. Hospital,
Near Mother Dairy Red Light Pandav Nagar Delhi-110092

With reference to our correspondence, Engineering College, Ajmer,N.H.8 , BARLIYA CIRCLE, NEAR NARELI TEMPLE, AJMER, is pleased to award this detailed Purchase Order to for supply of items as per the details given below at a total cost (Contract Value) **Rs. 307272(In Words:Three Lakh Seven Thousand Two Hundred Seventy Two Only)**

Sr. No	Item Name	Quantity	Place of Delivery	Installation Requirement (if any)
1	Logic Gate Trainer Kit	1	Engg. College, Ajmer N.H. 8,Barliya Circle, Near Nareli Temple, Ajmer	Onsite installation and testing & commissioning required.
2	Universal Logic Gate Trainer	1		
3	SOP and POS Trainer Kit	1		
4	Trainner Kit of Half adder/ Subtractor& Full Adder/ Subtractor (NAND & NOR gates)	1		
5	Trainer Kit to 4-bit ripple adder/ Subtractor (using basic Half adder/ Subtractor& basic Full Adder/ Subtractor).	1		
6	Trainer Kit of 4-to-1 multiplexer(using basic gates and verify the truth table. Also verify the truth table of 8-to-1 multiplexer using IC)	1		
7	Trainer Kit of 1-to-4 demultiplexer (To construct 1-to-8 demultiplexer using blocks of 1-to-4 demultiplexer)	1		
8	2x4 decoder Trainer Kit	1		

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9	Combinational Circuit Trainer Kit	1	Engg. College, Ajmer N.H. 8,Barliya Circle, Near Nareli Temple, Ajmer	Onsite installation and testing & commissioning required.
10	Flip- Flop Realistation Trainer Kit	1		
11	2, 4 & 8 asynchronous counter Trainer Kit	1		
12	Shift Register Trainer Kits	1		
13	Trainer Kit of BCD ripple counter	1		
14	4 Bit Ring counter Trainer Kit	1		
15	Trainer Kit of parallel in/Parallel out and Serial in/Serial out registers	1		
16	Bread Boards	10		
17	Function Genrator	10		
18	Multimeters	10		
19	Crocodile Clip 1	4		
20	DSO 30Hz	2		

Total price (without taxes) : Rs. 260400

Total applicable taxes : Rs. 46872

Total price (with taxes) : Rs. 307272

Total Octroi& Other Charges : Rs. 0

Delivery : Engineering College, Ajmer, N.H.8 , Barliya Circle, Near Nareli Temple, Ajmer

Testing/Installation Clause (if any): On site installation and testing & commissioning required. Price must be included in quotation.

Training Clause (if any) : N A

Technical Specifications : As per Annexure - 1

Delivery Period : 45 days or as early possible

Warranty (In Months): 36 Months from the date of successful acceptance of items.

Liquidated Damages : Liquidated Damages will be charged at the rate of 0.01 % per day on pre tax billing amount if delivery period exceeds 45 days. Purchase Order shall be understood cancelled automatically without any prior notification if delivery period exceeds 60 days.

Performance Security : Performance security amount Rs 13020 at the rate of (5 %) of the Total contract value to be submitted in form of Bank

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guarantee of any Nationalized. Bank only within 21 day from the date of issue of PO

Payment Terms : Below are the payment terms-

Satisfactory Delivery & Installation - 90% of total cost

Satisfactory Acceptance - 10% of total cost

Invoice Generation: The invoice has to be generated against GST No. **08AABAP0959P1ZZ** of Govt. Engineering College, Ajmer

Dr. U. S. Modani
Principal

Principal
Govt. Engineering College
AJMER

Govt. Engineering College, Ajmer
TEQIP-III

Accepted by Signature:

Date:

Address:

Annexure I

S. N.	Item Name	Specifications
1	Logic Gate Trainer Kit	* Realization of truth tables of AND, OR, NOT GATES, NAND, NOR and EX-OR GATES, using onboard IC's and (truth tables of logic gates: AND, OR, NOR, NAND, NOR, Ex-OR and Ex-NOR) * Logic Status Indicator. * Set of Patch chords * In-built Power Supply * User's Manual * House in an attractive ABS Plastic cabinet with cover
2	Universal Logic Gate Trainer Kit	* Realization of truth tables of AND, OR, NOT GATES, NAND, NOR and EX-OR GATES, using onboard IC's and the truth table of OR, AND, NOR, Ex-OR, Ex-NOR logic gates realized using NAND & NOR gates * Logic Status Indicator. * Set of Patch chords * In-built Power Supply * User's Manual * House in an attractive ABS Plastic cabinet with cover
3	SOP and POS Trainer Kit	* Boolean Function using logic gates in SOP & POS forms * Logic Status Indicator. * Set of Patch chords * In-built Power Supply * User's Manual * House in an attractive ABS Plastic cabinet with cover
4	Trainner Kit of Half adder/ Subtractor& Full Adder/ Subtractor (NAND & NOR gates)	* Study of Half Adder/Subtractor & Full Adder/Subtractor using NAND & NOR Gates and to verify their truth tables * Logic Status Indicator. * Set of Patch chords * In-built Power Supply * User's Manual * House in an attractive ABS Plastic cabinet with cover
5	Trainer Kit to 4-bit ripple adder/ Subtractor (using basic Half adder/ Subtractor& basic Full Adder/ Subtractor).	* Study of 4 bit ripple Adder/Subtractor using Basic Half Adder/Subtractor & Basic Full Adder/Subtractor using NAND & NOR Gates and realize * Circuit diagram printed onboard. * Set of Patch chords * In-built Power Supply * House in an attractive ABS Plastic cabinet with cover * User's Manual
6	Trainer Kit of 4-to-1 multiplexer(using basic gates and verify the	* Study of 4-to-1 Multiplexer using Basic Gates and Verify the truth table and 4-to-1 multiplexer using basic gates and verify the truth table. Also verify the truth table of 8-to-1 multiplexer using IC * Verify the truth table of 8-to-1 multiplexer using IC * Circuit diagram printed onboard. * Set of Patch chords

	truth table. Also verify the truth table of 8-to-1 multiplexer using IC)	* In-built Power Supply * House in an attractive ABS Plastic cabinet with cover * User's Manual
7	Trainer Kit of 1-to-4 demultiplexer (To construct 1-to-8 demultiplexer using blocks of 1-to-4 demultiplexer)	* Study of 1-to-4 De-multiplexer using Basic Gates and verify the truth table and design 1-to-4 demultiplexer using basic gates and verify the truth table. Also to construct 1-to-8 demultiplexer using blocks of 1-to-4 demultiplexer * To construct 1-to-8 demultiplexer using blocks of 1-to-4 de-multiplexer * Circuit diagram printed onboard. * Set of Patch chords * In-built Power Supply * House in an attractive ABS Plastic cabinet with cover * User's Manual
8	2x4 decoder Trainer Kit	* Study of 2x4 decoder using basic gates and verify the truth table. also verify the truth table of 3x8 decoder using IC and design 2x4 decoder using basic gates and verify the truth table. Also verify the truth table of 3x8 decoder using IC * Circuit diagram printed onboard. * Set of Patch chords * In-built Power Supply * House in an attractive ABS Plastic cabinet with cover * User's Manual
9	Combinational Circuit Trainer Kit	* Study, design & realize a combinational circuit that will accept a 2421 BCD Code and Drive a til -312 seven-segment display and * Circuit diagram printed onboard. * Set of Patch chords * In-built Power Supply * House in an attractive ABS Plastic cabinet with cover * User's Manual
10	Flip- Flop Realistation Trainer Kit.	* Study of Basic Logic Gates, Realize the R-S, J-K and D-Flip Flops with and without clock signal and verify their truth table.and Using basic logic gates, realize the R-S, J-K and D-flip flops with and without clock signal and verify their truth table) * Circuit diagram printed onboard. * Set of Patch chords * In-built Power Supply * House in an attractive ABS Plastic cabinet with cover * User's Manual
11	2, 4 & 8 asynchronous counter Trainer Kit	* Study of construct a divide by 2, 4 & 8 asynchronous counter. Construct a 4-bit Binary Counter and Ring Counter for a particular output pattern using d Flip Flop. * Circuit diagram printed onboard. * Set of Patch chords * In-built Power Supply

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		* House in an attractive ABS Plastic cabinet with cover * User's Manual
12	Shift Register Trainer Kit	* To design and construct unidirectional shift register and verify the function * Circuit diagram printed onboard. * Set of Patch chords * In-built Power Supply * House in an attractive ABS Plastic cabinet with cover * User's Manual
13	Trainer Kit of BCD ripple counter	* To design and construct BCD ripple counter and verify the function * Circuit diagram printed onboard. * Set of Patch chords * In-built Power Supply * House in an attractive ABS Plastic cabinet with cover * User's Manual
14	4 Bit Ring counter Trainer Kit	* To design and construct a 4 bit ring counter and verify the function * Circuit diagram printed onboard. * Set of Patch chords * In-built Power Supply * House in an attractive ABS Plastic cabinet with cover * User's Manual
15	Trainer Kit of parallel in/Parallel out and Serial in/Serial out registers	* To perform input/output operations on parallel in/parallel out and serial in/serial out registers using clock. also exercise loading only one of multiple values into the register using multiplexer. * Circuit diagram printed onboard. * Set of Patch chords * In-built Power Supply * House in an attractive ABS Plastic cabinet with cover * User's Manual
16	Bread Board	Bread Board (BB-2T3D) (Dimensions: 101.5×165.5×8.5mm 2 Terminal Strip: 1260 Tie-point, 4 Distribution strips: 300 Tie-point 3 Binding Posts ABS plastic material Black Metal Plate: 130x216x1mm Copper nickel plated spring clips Accepts a variety of wire sizes (20~29 AWG) Voltsge / current : 300V / 3~5 A)
17	Function Generator	* Frequency Range : 0.01Hz-1MHz in decadic steps. Sine, Square, Triangle, Sawtooth/Ramp and Pulse TTLOutput and facility of DC offset. * Display Freq Volt (Vp) : Digital (4 Digit 7 Segment display). * Accuracy : Better than ± (1% 1 digit) of F.S. ±3% (50W impedance). * Amplitude : upto 30V p-p. (variable) by coarse and fine control * Step attenautor : 20dB and 40dB steps. * DC Offset : Upto ±10V into open circuit. * Output Impedance : 50W & 600W ± 10%.
18	Multimeter	Type Ac/DC voltage 200mV/20V/200V/200V,DC current 200μA/2mA/20mA/2mA/20mA/200mA/10A,Resistance200Ω/2KΩ20KΩ/200KΩ2MΩ,Temperature© -20°C/400°C1000°C .
19	CRO	* Bandwidth : AC 10Hz ~ 30MHz (-3dB) DC ~ 30MHz (-3dB) * Y Deflection : 5mV / div ~ 20V / div

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		* Rise Time : <18ns, Mag x 5 Accuracy : <5% * Max Input : 400V(DC+ACp-p) * Sweep Mode : Auto, Trig, Lock, Single * Sweep Rate : 0.1μs/div ~ 0.2s/div l-2-5 20 steps, error ±5% * Trig Source : Y1, Y2, ALT, Line, Ext, TV-H, TV-V * Min Sync. Level : Trig DC ~ 30MHz, Int. 1 div, Ext. 0.2Vp-p, TV Int. 2div, Ext. 0.3Vp-p Trig Lock (50Hz ~ 10MHz) Internal 2div * Freq. Response : AC : 10Hz ~ 1MHz -3dB DC : 0 ~ 1MHz -3dB * Z Max. Input : 400V (DC+ACp-p) * Min Input Level : TTL Level * Wave Form : Square wave * Amplitude : 1KHz ±2% * Frequency : 0.5Vp-p ±2% * Standard Accessories : Power Chord, Two 30 MHz Oscilloscope Probes, Manual
20	DSO	* Bandwidth : 30 MHz * Sample Rate : 250 MS/s * Horizontal Scale(S/div) : 4ns/div~100s/div, step by1~2~4 * Rise time : ≤14ns * Display : 8" Color LCD,TFT display, 800x600 pixels, 65535 colors * Channel : 2 + 1 (External) * Record Length : Max 10 K * Input Coupling : DC, AC, Ground * Input impedance : 1MΩ±2%, in parallel with 15pF±5pF * Channels Isolation : 50MHz: 100 : 1, 10MHz: 40 : 1 * Max. input voltage : 400V (PK-PK) (DC + AC PK-PK) * DC gain accuracy : ±3% * DC accuracy : Average≥16: ±(3% reading + 0.05 div) for ΔV * Probe attenuation factor : 1X, 10X, 100X, 1000X * LF respond(AC, -3dB) : ≥5Hz (at input, AC coupling, -3dB) * Waveform storage : 15 waveforms * Lissajous figure - Bandwidth : Full bandwidth, - Phase difference : ±3 degrees * Communication interface : USB, USB flash disk storage, Pass/Fail, LAN, VGA (optional) * Cymometer : Available * Power supply : 100V-240V AC, 50/60HZ,CAT II * Power consumption : < 18W * Fuse : 2A, T class, 250V * Battery : Not support

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Annexure 2 (Purchase Order)

PERFORMANCE SECURITY FORM

To: _____ (Name of Purchaser)

WHEREAS ..... (Name of Supplier) hereinafter called "the Supplier" has undertaken , in pursuance of Contract (Notification of Award) No..... dated,..... 2019 to supply..... .....(Description of Goods and Services) hereinafter called "the Contract".

AND WHEREAS it has been stipulated by you in the said Contract that the Supplier shall furnish you with a Bank Guarantee by a Nationalized bank for the sum specified therein as security for compliance with the Supplier's performance obligations in accordance with the Contract.

AND WHEREAS we have agreed to give the Supplier a Guarantee:

THEREFORE WE hereby affirm that we are Guarantors and responsible to you, on behalf of the Supplier, up to a total of ..... (Amount of the Guarantee in Words and Figures) and we undertake to pay you, upon your first written demand declaring the Supplier to be in default under the Contract and without cavil or argument, any sum or sums within the limit of ..... (Amount of Guarantee) as aforesaid, without your needing to prove or to show grounds or reasons for your demand or the sum specified therein.

This guarantee is valid until the .....day of.....2019.

Signature and Seal of Guarantors

Date.....2019.
Address:.....
.....
.....

Note: *The Bank Guarantee to be issued by nationalized bank only and is to be submitted on a non-judicial stamp paper of Rs. 100/- (One Hundred only). The non-judicial stamp paper should be purchased in the name of issuing bankers. The Issuing bank must provide its Head Office/Regional office addresses of communication*